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Zinc Incorporation via the Vapor−Liquid−Solid Mechanism into InP Nanowires

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Semiconducting nanowires[1,2] hold the promise of combining III−V materials with silicon technology.[3−5] For most applications it is essential to incorporate dopant impurities in the nanowire. However, the mechanism for impurity doping via the vapor−liquid−solid (VLS) mode[6] is not yet understood. It remains unclear whether dopants are incorporated via the catalyst particle (VLS) or directly from the gas phase via a vapor−solid (VS) mechanism, since during VLS growth competitive sidewall growth (VS) may also occur. For silicon nanowires, axial dopant modulations have been shown,[7] indicating dopant incorporation via the catalyst particle. For germanium and III−V core/shell nanowires, controllable dopant incorporation via a VS mechanism (shell deposition) has been shown.[8−12] In this communication we demonstrate that it is also possible to incorporate zinc dopant atoms into an indium phosphide (InP) nanowire directly via the VLS mechanism. We show this by growing InP nanowires with an axial pn-junction. After growth the wires are etched radially to remove the shell and contacted electrically. Electrical characterization leads to the conclusion that the dopant atoms are incorporated into the InP lattice via the VLS mechanism. We believe that this has major implications for future applications, since controlling dopant incorporation via both the catalyst particle and sidewall deposition gives the ultimate freedom of design.

Indium phosphide nanowires were grown by means of metal−organic vapor-phase epitaxy (MOVPE)[13] in the VLS-mode using 50 nm gold colloids as catalyst particles deposited on n-type phosphorus-terminated InP (111) substrates. The precursor gases used were trimethylindium (TMI) and phosphine (PH_3). Dopants were introduced using diethylzinc (DEZn) for p-type and H_2S for n-type. Recently it has been shown that Zn-doped MOVPE-grown InP nanowires exhibit a (periodically twinned) zinc-blende crystal structure, when $p_{DEZn} > 5 \times 10^{-5}$ mbar (10^{18} cm^{-3}),[14] and S-doped InP nanowires have a wurtzite crystal structure. A typical transmission electron micrograph (TEM) image is shown in Figure 1a. In this particular case, a p-type section was grown on top of the n-type section. Figure 1a−d indicate that, as observed before,[14] the p-type (zinc-blende) segment has {111} side facets and the n-type part (wurtzite) has $\{100\}_h$ side facets. When such an axial pn-junction is grown intentionally, a radial pn-junction is formed unintentionally by competitive VS growth at the bottom of the wire. To remove this undesired radial pn-junction, a wet-chemical etch using $H_2SO_4/H_2O_2/H_2O$ = 3:1:1 at room temperature was performed. Results

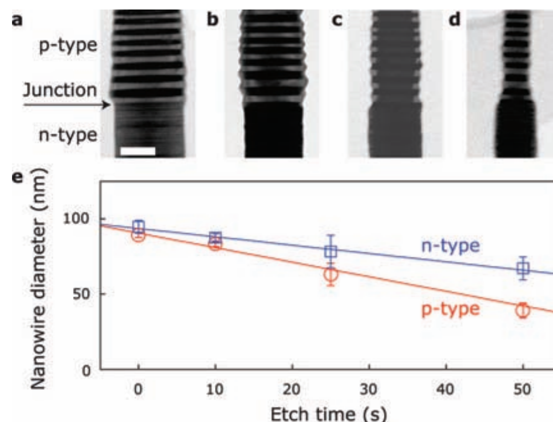

Figure 1. (a) Transmission electron micrograph (TEM) of an as grown nanowire pn-junction. The position of the junction is indicated by the arrow. The n-type part is below the arrow, and the p-type part is above. (b−d) TEM image of a nanowire etched for 10 (b), 25 (c), and 50 s (d). Scale bar is 50 nm for all panels. (e) Diameter as a function of etch time for both the n-type part (blue squares) and the p-type part (red circles). The solid curves are linear fits.

are shown in Figure 1b, c, and d for 10, 25, and 50 s etching times, respectively. These TEM images clearly show a different etch rate for the top (p-type) and bottom (n-type) sections of the wire. This behavior is made quantitative in Figure 1e, in which the average diameter is plotted against the etching time. Each data point is an average of measurements on at least five nanowires. The diameter of the n-type segment was measured at the junction, while the diameter of the p-type segment was measured 100 nm from the junction, since close to the junction the etching rate is enhanced, probably by an excess of etchant supplied from the n-type side where the etch rate is lower. The etch rate for the n-type material is about a factor of 2 slower (0.28 ± 0.09 nm/s) than that for the p-type material (0.49 ± 0.05 nm/s). Etching of InP in acidic H_2O_2 solution is, like etching of GaAs,[15] due to a chemical (and not an electroless) mechanism. Chemical etching is expected to be anisotropic.[16] The difference in chemical etch rates of the wurtzite and zinc-blende segments most probably originates from the different natures of the side facets.

To investigate if dopants were still present after etching, the wires were contacted and measured electrically. This was done in a vertical configuration, using a similar scheme as reported in refs 17−19 and is depicted schematically in Figure 2. The wires were first etched for 10 s (Figure 2-2). The diameter of the p-InP segment after etching is almost equal (80 nm) to the nanowire diameter determined by the VLS mechanism, measured just below the top, showing that the shell has essentially been removed. Subsequently,

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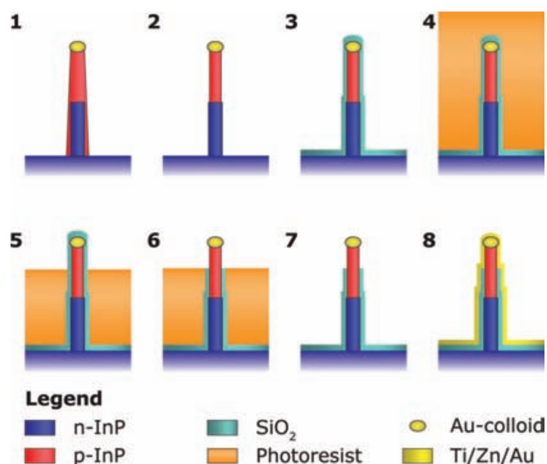

Figure 2. Schematic cross sections illustrating the main process steps for fabricating vertical pn-junctions. Different colors are explained in the legend, and the different process steps are explained in the text.

a 300 nm PECVD SiO_2 layer was deposited uniformly over the substrate and the nanowires (3). A photoresist layer was spun on, so that the nanowires were completely buried in the photoresist (4). A controlled etch-back step using an O_2 plasma was performed to thin down the photoresist layer until 300 nm of the nanowires were uncovered (5). Then the SiO_2 around the top of the nanowire was removed by a wet etching step in a buffered HF solution (6), after which the photoresist layer was removed (7). Finally, a top Ti/Zn/Au contact was patterned using a standard lift-off technique (8) after which a rapid thermal anneal step was performed. An SEM image of a nanowire device before metal deposition is shown in the inset of Figure 3a.

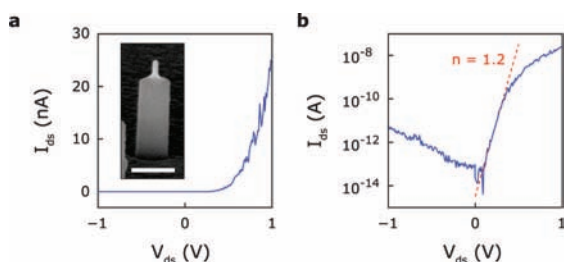

Figure 3. (a) Typical current−voltage characteristic of a vertical nanowire pn-junction. Inset shows a scanning electron micrograph of a nanowire with a wrapped SiO_2 layer and the top opened up, corresponding to schematic 7 in Figure 2. Scale bar is 500 nm. (b) Current−voltage characteristic on a logarithmic scale, showing an ideality factor of $n = 1.2$ and a rectification of 4 orders of magnitude.

A typical current−voltage curve of a device with four wires in parallel is shown in Figure 3. In this measurement the voltage to the top contact was swept, while the bottom contact was grounded. The nanowires show clear diode behavior (current increases in forward direction), indicating a pn-junction. An ideality factor of $n = 1.2$ is obtained from the slope of the onset of the forward current, which is close to that of an ideal p-n junction ($n = 1$). The top contact to the p-type part of the nanowire is not ohmic. However, the rectifying behavior cannot originate from this Schottky contact, since this contact is in reverse for this polarization.[20] This top contact actually limits the forward current. From electrical measurements on vertically contacted uniformly doped n-type InP nanowires grown on the same substrates, we know that the substrate contact is ohmic, due to the large contact area and the high dopant concentration (10^{19} cm^{-3}) of the substrate. Similar wires have been detached from the surface and were contacted individually by e-beam lithography in a horizontal configuration.[11] These wires show electroluminescence in the forward direction, confirming our assumption that the pn-junction provides the rectifying behavior. These experiments demonstrate that the core of the wire contains ionized Zn atoms and that these atoms are incorporated into the InP lattice via the VLS mechanism.

In conclusion, we demonstrate that zinc atoms incorporate into InP nanowires through the catalyst particle by successfully fabricating InP nanowire diodes. After using a chemical etch to selectively etch the p-type shell, originating from sidewall deposition, we still observe diode behavior, illustrating that the Zn atoms are also present in the core of the nanowire.

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